ANALOG IC DESIGN USING CADENCE

Event No	EC058
Organizing Department	Electronics and Communication Engineering
Associate Dept. | NSC	Institution of Electronics and Telecommunication Engineering International Society for Technology in Education
Date	23/03/2023 to 25/03/2023 (3 Days)
Time	08:45 AM to 04:15 AM
Event Type	VAC / Training Program
Event Level	Dept. Level
Venue	VLSI LAB
Total Participants	50
Students - Internal	50

Related SDG

Involved Staffs

Sl	Name	Role
1	Muralidharan J	Coordinator
2	Prasad J	Coordinator

Outcome

At the conclusion of the course, the students are able to identify basic building blocks in analog integrated circuits, analyze performance parameters such as delay and power. Also the students are able to design analog ICs of small to medium complexity and verify them using CADENCE EDA simulation tools.

Event Summary

In the past two decades, CMOS technology has rapidly embraced the field of analog integrated circuits, providing low cost, high performance solutions and rising to dominate the market. The CMOS processes have emerged as a viable choice for the integration of today's complex mixed signal and SOC systems. Analog circuit design has evolved with the technology moving from high voltage, high power small scale analog circuits to low voltage, low power ultra large scale circuits. Analog IC design generally involves more personalized focus into each circuit, and even the sizing and specifics of each transistor. Also, many foundry processes are primarily developed for digital ICs with analog features, which requires analog IC designers to work with process constraints and features better suited to digital ICs. Cadence circuit design solutions enable fast and accurate entry of design concepts, which includes managing design intent in a way that flows naturally in the schematic. The value added course on Analog IC design using CADENCE is started with introduction to analog circuits. The operation and characteristics of the analog circuits were taught during the first day of the course. Later on the CADENCE EDA tool demonstration was carried for basic circuits to make the students understand the usage of the tool. The next day the students are instructed to design fundamental circuits using CADENCE EDA tools to have a hands on training. Then various performance analyzing parameters were taught in the post students hands on session. The assessment is carried out for the students based on the learning carried out in the course.

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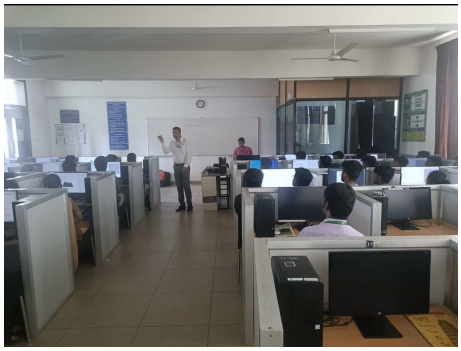

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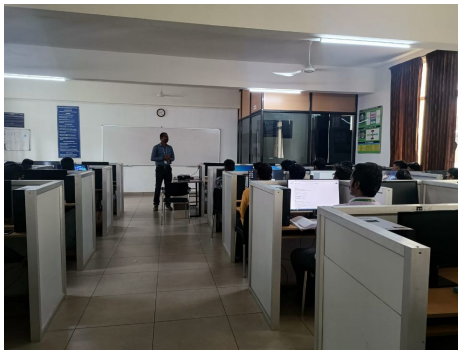

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